

DESCRIPTION:

This document describes Aplus 256M x 72-bit 2GB DDR2 SDRAM (Synchronous DRAM) ECC memory module. The components on this module include thirty-six 128M x 4-bit (4Banks) DDR2 SDRAM in FBGA packages. This 240-pin Fully Buffered DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

FEATURES:

- JEDEC standard Double data rate2
- 1.8V \pm 0.1V Power supply for DRAM VDD/VDDQ
- 1.5V +0.075/-0.045V Power supply for AMB VCC
- 3.3V \pm 0.3V Power supply for VDDSPD
- All inputs and outputs are compatible with SSTL_1.8 interface
- Host interface and AMB component industry standard compliant
- High-speed differential point-to-point link at 1.5volt
- Link transfer rate 3.2Gb/s, 4.0Gb/s
- Programmable Burst length 4/8 with both sequential and interleave mode
- 8192 refresh cycles / 64ms
- OCD (Off-chip driver impedance adjustment)
- ODT (On-die termination)
- MBIST IBIST test functions
- Serial presence detect with EEPROM

DDR2 DRAM Speed

- DDR2-667 667Mbps CL-tRCD-tRP (5-5-5)
- DDR2-533 533Mbps CL-tRCD-tRP (4-4-4)

PERFORMANCE:

- Clock Cycle Time (tCK) CL(5) 3ns (min.) /8ns (max.)
- Clock Cycle Time (tCK) CL(4) 3.75ns (min.) /8ns (max.)
- Row Cycle Time (tRC) 60ns (min.)
- Refresh Row Cycle Time (tRFC) 105ns (min.)
- Row Active Time (tRAS) 45ns (min.)
- Operating Temperature 0°C ~ 95°C
- Storage Temperature -55°C ~ +100°C



