

Description

This document Aplus 128M x 64-bits DDR2-667 CL5 SDRAM (Synchronous DRAM).memory module. The components on this module include eight 128Mx8bits DDR2 SDRAMs FBGA packages.This 240-pin DIMM use gole contacy finger and requires +1.8v.The electrical and mechanical specification are as follows:

Features

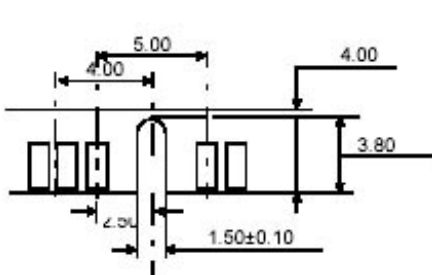
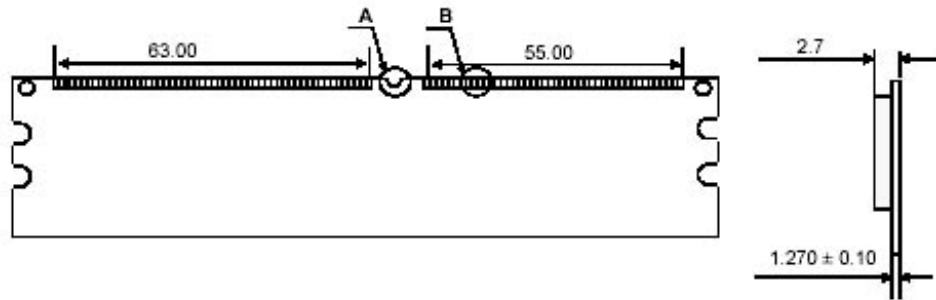
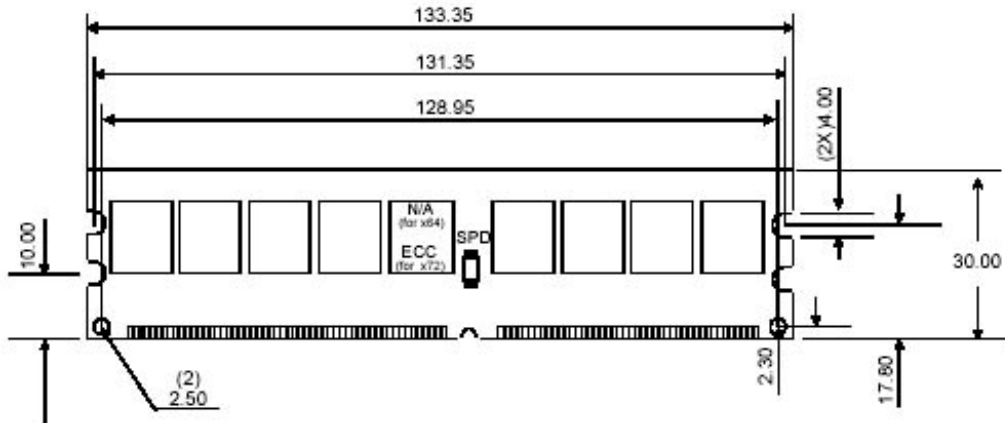
- 240-pin, unbuffered dual in-line memory module
- VDD = VDDQ = 1.8V
- VDDSPD = 1.7–3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Halogen-free
- Gold edge contacts
- Single rank

Options

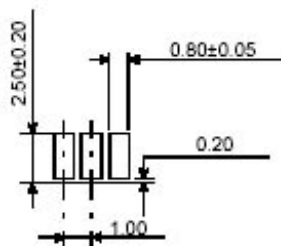
- Operating temperature
 - Commercial (0°C ≤ TA ≤ +70°C)
 - Industrial (−40°C ≤ TA ≤ +85°C)

Industry Nomenclature	Data Rate (MT/s)			tRCD (ns)	tRP (ns)	tRC (ns)	Memory Clock/ Data Rate	Clock Cycles (CL-tRCD-tRP)
	CL = 5	CL = 4	CL = 3					
PC2-5300	667	553	400	15	15	60	3.0ns/667 MT/s	5-5-5

240-Pin DDR2 UDIMM



Detail A



Detail B

